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10ES32

Third Semester B.E. Degree Examination, June/July 2014
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With respect to a semiconductor diode, explain the following:
   i) Transition and diffusion capacitance.
   ii) Reverse recovery time. **(06 Marks)**

b. Explain the operation of the circuit shown in Fig.Q.1(b). Draw output waveform and transfer characteristic. [Assume ideal diode]. **(07 Marks)**

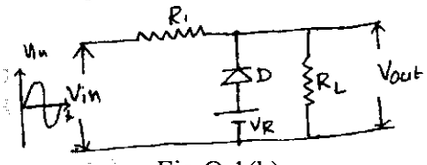

Fig.Q.1(b)

c. Write the procedure for analyzing the clamping circuit. Determine output voltage for the network shown in Fig.Q.1(c). Assume f= 1000Hz and ideal diode. **(07 Marks)**

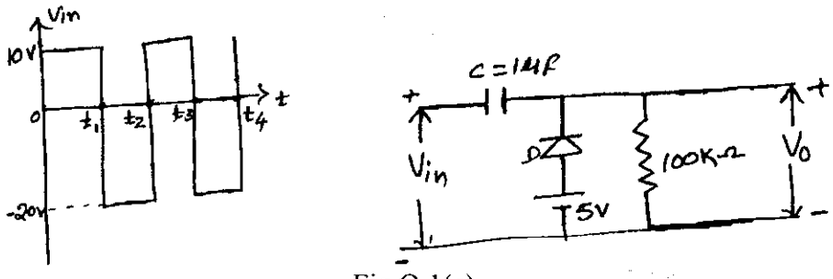

Fig.Q.1(c)

2 a. What is biasing? Discuss the factors causes for bias instability in a transistor. **(06 Marks)**

b. With circuit diagram, explain Emitter stabilized bias circuit. Write the necessary equation. **(07 Marks)**

c. For the circuit shown in Fig.Q.2(c), find I_C, V_B, V_E, R_1 and $S_{(ICO)}$. **(07 Marks)**

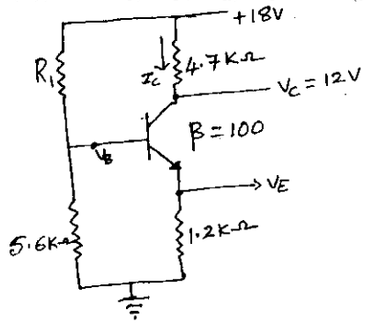

Fig.Q.2(c)

3 a. Draw the circuit diagram of common Emitter fixed bias configuration. Derive the expression for Z_i, Z_o, A_v using re model. **(08 Marks)**

b. For the network shown in Fig.Q.3(b), determine r_e, Z_i, Z_o, A_v and A_I. **(06 Marks)**

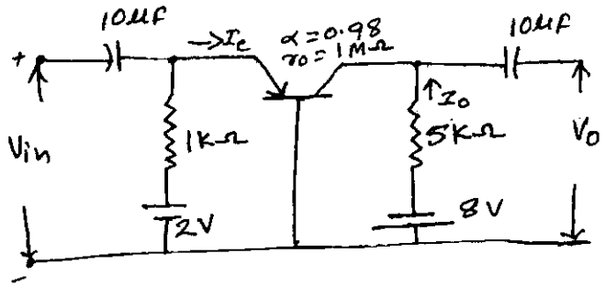

Fig.Q.3(b)

c. What are the advantages of h-parameters? **(06 Marks)**

4 a. Discuss the effect of various capacitors on frequency response. **(04 Marks)**

b. What is Miller effect? Prove that Miller effect capacitance $C_{mi} = (1 - A_v) C_f$ and $C_{mo} = \left(1 - \frac{1}{A_v}\right) C_f$. **(08 Marks)**

c. Determine the high frequency response of the amplifier circuit shown in Fig.Q.4(c). Draw the frequency response curve. **(08 Marks)**

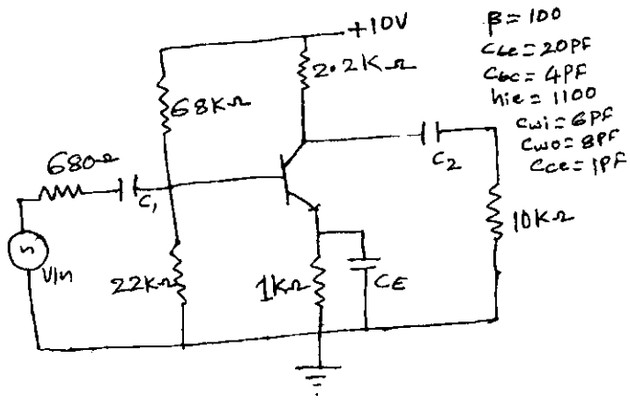

Fig.Q.4(c)

PART – B

5 a. Explain the need of cascading amplifier? Draw and explain the block diagram of two-stage cascade amplifier. **(04 Marks)**

b. With block diagram, explain the concept of feedback amplifier. If an amplifier has mid-band voltage gain (A_v mid) of 1000 with f_L = 50Hz and f_H = 50 kHz, if 5% feedback is applied then calculate f_L and f_H with feedback. **(08 Marks)**

c. Derive the expression for input resistance (R_{if}) for feedback amplifier employing current-series feedback. **(08 Marks)**

6 a. A series fed class-A amplifier shown in Fig.Q.6(a) operates from dc source and applied sinusoidal input signal generates peak base current 9 mA. Calculate I_{CQ}, V_{CEQ}, P_{DC}, P_{ac} and efficiency. Assume $\beta = 50$ and $V_{BE} = 0.7V$. **(06 Marks)**

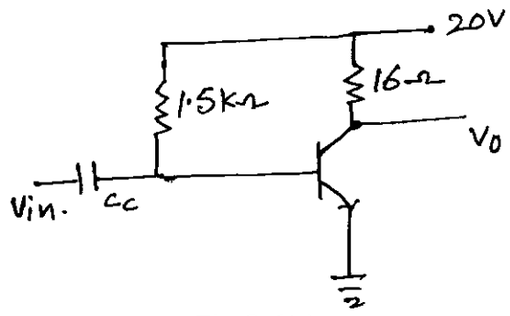

Fig.Q.6(a)

b. What is harmonic distortion? Explain the three point method of calculating the second harmonic distortion. **(08 Marks)**

c. Explain the working of complementary symmetry class-B amplifier. **(06 Marks)**

7 a. With circuit diagram, explain RC-phase shift oscillator using BJT. **(08 Marks)**

b. In a transistorized Hartley oscillator the two inductances are 2mH and 20μH, while the frequency is to be changed from 950kHz to 2050 kHz. Calculate the range over which the capacitor is to be varied. **(04 Marks)**

c. With circuit diagram, explain the working principle of crystal oscillator in series resonant mode. A crystal has the following parameters L = 0.334H, C = 0.065pF and R = 5.5KΩ. Calculate the resonant frequency. **(08 Marks)**

8 a. Compare FET over BJT. **(06 Marks)**

b. With equivalent circuit obtain the expression for Z_i and Z_o for JFET self bias with unbypassed R_s. **(08 Marks)**

c. The fixed bias configuration shown in Fig.Q.8(c) has $V_{GSQ} = -2V$, $I_{DQ} = 5.625mA$ with $I_{DSS} = 10mA$, $V_p = -8V$ and $Y_{DS} = 40\mu s$ determine g_m, r_d, Z_o and A_v. **(06 Marks)**

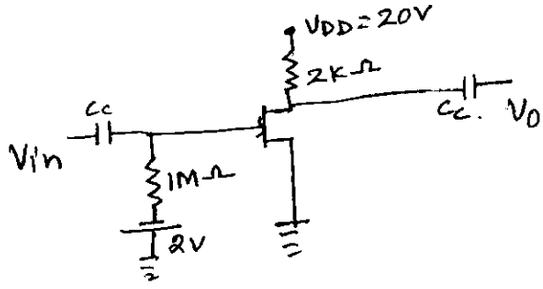

Fig.Q.8(c)

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